FET power amplifier boosts transmitter efficiency

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☐ Most of the power needed to drive a radio transmitter is consumed in the power amplifier. For that reason, the efficiency of the power amplifier determines the battery and heat-sink requirements of portable communications equipment and rescue beacons. Increasing this efficiency can improve performance, increase operating life, or decrease the size and weight of a transmitter.

The high-frequency power amplifier described here operates in the class F mode for high output efficiency and exploits the negligible drive-power requirement of a field-effect transistor. The prototype produces a maximum of 330 milliwatts with 73% efficiency at 25 megahertz. This design won an award in the 1974 double-diffused-MOS contest sponsored by Signetics Corp. while the author was with Cincinnati Electronics Corp.

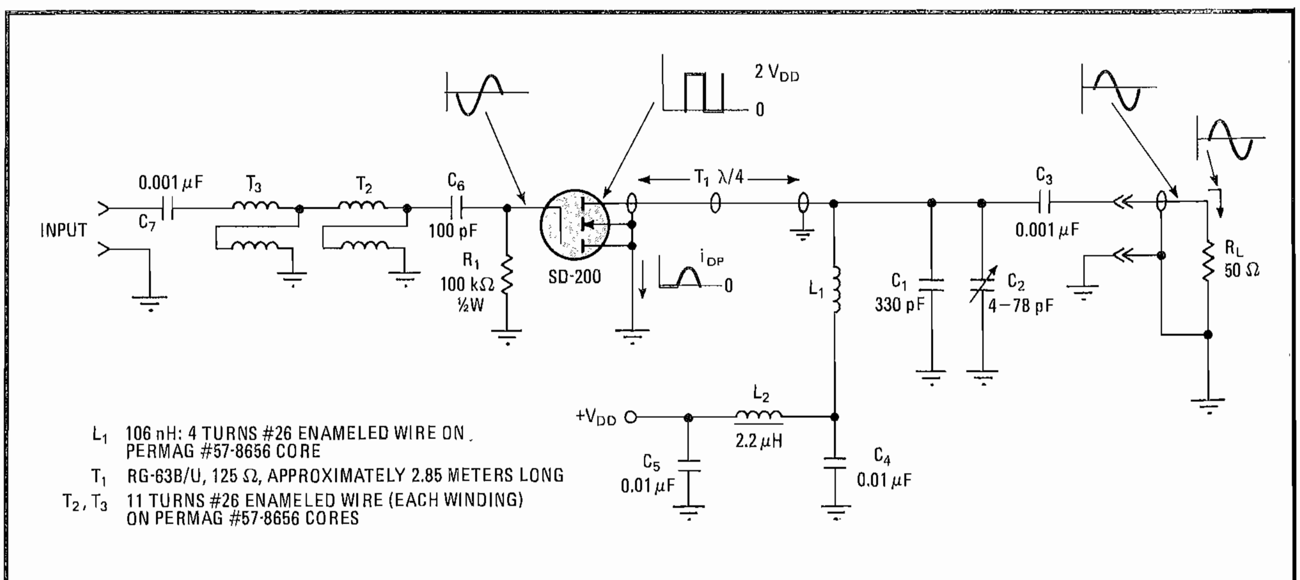
As shown in Fig. 1, the amplifier uses a single FET or a pair of FETs in parallel, driven to act as a switch. The parallel-tuned output circuit acts as a short circuit to all harmonics of the signal frequency, but the impedance transformation produced by the quarter-wavelength transmission line causes the drain to see a short circuit for the even harmonics and an open circuit for the odd harmonics.

This combination of impedances produces a square-wave drain voltage and a half-sine-wave drain current. Since the drain voltage is near zero while drain current is flowing, the FET dissipates very little power. This mode of operation, designated class F, could ideally be 100% efficient and thus provide 27% more output power and 27% greater efficiency than class B operation (see F. H. Raab, "High efficiency amplification techniques," IEEE Circuits and Systems Journal, 1975, vol. 7, no. 10, pp. 3–11).

The Signetics SD-200 is well suited to this application because it can operate as a switch at frequencies that reach into the very-high-frequency region. To operate the FET as a switch, more voltage is applied to the gate than is necessary to sustain the current flowing in the drain. Since the drain current is sinusoidal when it is not zero, a sinusoidal gate voltage of sufficient amplitude causes switching. What's more, because the gate voltage is sinusoidal and gate current is negligible, this amplifier can be driven directly by the radio-frequency oscillator or frequency multiplier. This capability eliminates components and reduces power consumption.

Transmission line boosts efficiency

Figure 2 depicts an equivalent circuit for the amplifier shown in Fig. 1; the FET is replaced by a switch and a series saturation resistance R_{on}. The switch opens and closes at the signal frequency. Load resistor R_L is shunted by a tank circuit that has infinite impedance at



1. High efficiency. A microwave field-effect transistor acts as a high-speed switch in a highly efficient rf power amplifier that operates in the hf region. A quarter-wave transmission line produces the desired impedances for multiresonator class F operation. Without the quarter-wave line, the amplifier would operate in the class B mode. This circuit operates at 25 MHz and delivers 330 mW into a 50-ohm load.

the signal frequency and zero impedance at all harmonics. The impedance presented to the drain by the transmission line therefore depends on the frequency. At the fundamental frequency, the transmission line is a quarter-wave transformer; its input impedance is:

$$R = R_o^2/R_L$$

where R_o is the characteristic impedance of the line. At the even harmonics, the line acts as if it were a half-wavelength long and reproduces the short-circuited output at the drain. At the odd harmonics, it acts as a quarter-wavelength line, converting the shorted output into an open circuit at the drain. This set of impedances is the key to high-efficiency operation.

The FET is driven so that it is turned on to act like a closed switch half of the time and turned off to operate as an open switch half of the time. When the FET is driven on, the drain voltage must be zero. The short circuits for the even harmonics require that only the fundamental and its odd harmonics be present in the drain-voltage waveform. These components combine to produce a square-wave drain voltage.

Since the average voltage on the drain must be V_{DD} so that there is no dc drop in the rf choke, the square wave has levels of 0 and $+2V_{DD}$. To simplify the discussion, the characteristic impedance of the line is assumed to be the same as the load resistance, so that R and R_o are equal to R_L, and R_{on} is assumed to be zero. The fundamental-frequency component of the square-wave drain voltage then appears across the load:

$$v_L(t) = (4V_{DD}/\pi) \sin\omega t$$

Incidentally, this voltage lags the drain voltage by 90° because of the phase shift in the quarter-wave transmission line.

The fundamental-frequency current that flows in the load is just the load voltage divided by R:

$$i_L(t) = (4V_{DD}/\pi R) \sin\omega t$$

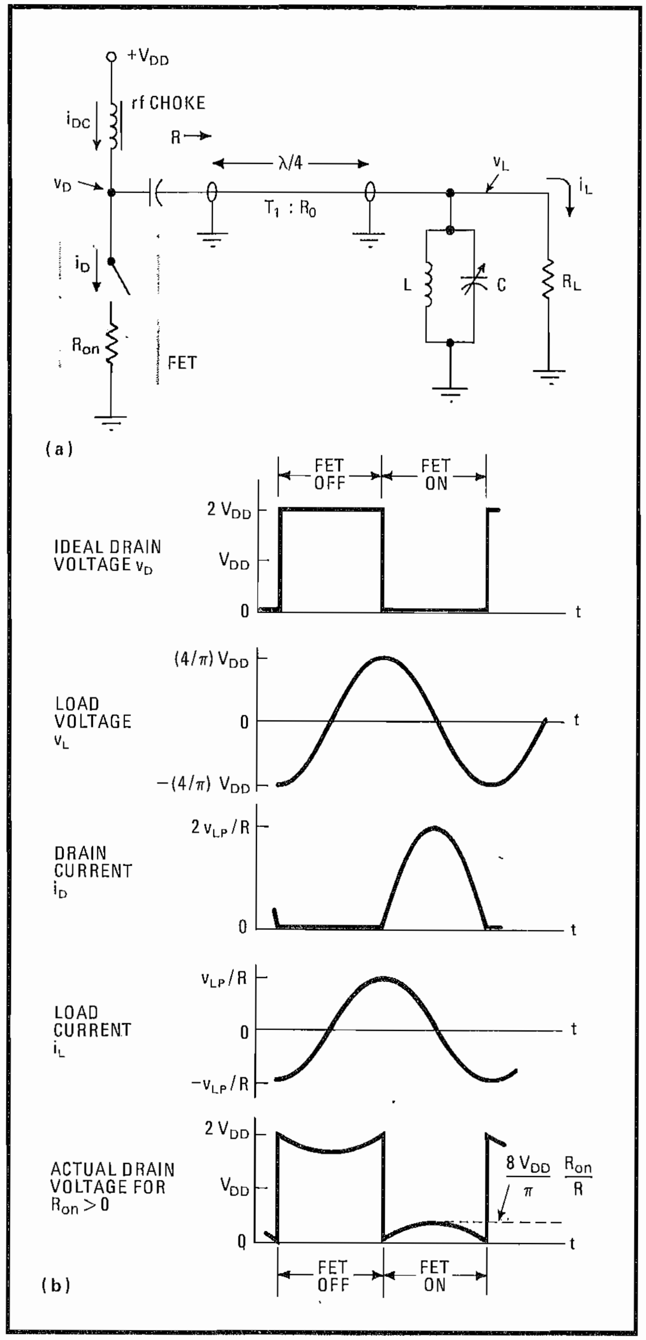
The odd harmonics in the drain-voltage waveform convert the sine wave into a square wave, but since they do not cause current to flow, they consume no power. The output power is produced entirely by the fundamental-frequency current and voltage:

$$P_o = \tfrac{1}{2} v_{LP} i_{LP} = 8V_{DD}^2/\pi^2 R$$

When the FET is off, the drain current must be zero. The rf choke passes only dc, so the fundamental-frequency current that flows through the load must also flow through the drain. Since the transmission line is an open circuit to odd harmonics, the drain current must be composed of a fundamental and even harmonics. Furthermore, because the transmission line acts as a short circuit to even harmonics, the drain can draw any amount of even-harmonic current necessary to meet other circuit requirements. This even-harmonic current results in a half-sinusoidal drain current whose peak amplitude is equal to the peak-to-peak amplitude of the output current:

$$i_{DP} = 8V_{DD}/\pi R$$

The even-harmonic currents circulate through the drain, transmission line, and output network, but no power is consumed because they produce no voltages.



2. Here's how. Equivalent circuit (a) and waveforms for voltages and currents (b) show operation of class F amplifier. Switching action of FET produces square drain-voltage wave, but tuned circuit and transmission line remove harmonics to produce sinusoidal outputs. Values on curves are for case of $R_o = R_L = R$.

The dc input required is the average drain current, which is obtained by dividing i_{DP} by π:

$$i_{DC} = 8V_{DD}/\pi^2 R$$

Multiplication of i_{DC} by V_{DD} gives the input power as $8V^2_{DD}/\pi^2 R$; since this is the same as the expression for output power, the efficiency of the ideal class F amplifier is 100%. This result is also apparent from the drain voltage and current waveforms in Fig. 2b. When drain current is not zero, drain voltage is zero, and when drain voltage is not zero, drain current is zero. Consequently, no power is consumed by the device.

Saturation resistance lowers efficiency

In a real FET, saturation resistance R_{on} is greater than zero and, therefore, the device consumes some power, reducing the efficiency of the amplifier below 100%. The output voltage and current must be sinusoidal, however, and the drain current must be half-sinusoidal. This drain current, flowing through the saturation resistance, causes the bottom of the drain voltage to differ from a square wave by a half-sinusoid with a peak value $i_{DP} R_{on}$, or $2v_{LP}R_{on}/R$, as shown in Fig. 2b.

Since there can be no even harmonics in the drain-voltage waveform, the half-sinusoidal droop also appears in the top part of the waveform. This droop reduces the output voltage because it acts in opposition to the fundamental component of the ideal square wave. The resulting output voltage across the load can be determined by equating the fundamental component of the drooping drain voltage and the output:

$$v_{LP} = (4V_{DD}/\pi)[R/(R+2R_{on})]$$

When this equation is used in the expressions for drain current, dc current, output power, and input power, the efficiency of the class F amplifier is found to be:

$$\eta_F = R/(R+2R_{on})$$

Maximizing the power

In a reliable amplifier circuit, the peak voltage and peak current should not exceed the ratings of the FET. For the SD-200, these are 25 V and 50 mA, respectively; therefore, V_{DD} must not exceed 12.5 V, and i_{DC} must not exceed 15.9 mA for a single device or 31.8 mA for two devices in parallel.

Maximum power output is obtained by choosing the load line R so that maximum drain current is reached when the maximum supply voltage is applied. This value of R is:

$$R_{MP} = (8V_{DD\,MAX}/\pi i_{DP\,MAX}) - 2R_{on}$$

If the saturation resistance R_{on} were zero, the optimum resistance would be 637 Ω, yielding an output of 198 milliwatts. Saturation resistance reduces not only efficiency, but also the maximum power. For the typical R_{on} of 40 ohms, R_{MP} becomes 637 − 80 or 557 ohms. The efficiency is therefore:

$$\eta_F = 557/637 = 87.5\%$$

A single device with typical saturation resistance can thus produce about 173 mW.

Assessing actual performance

A working model of the circuit in Fig. 1 is shown in Fig. 3a. Transformer T_1 used a 125-ohm transmission line simply because it was available; however, its load line produces nearly maximum power for a parallel pair of FETs. Although it may seem crude to use such a large coaxial cable with such a small device, the same load could have been produced with a pi-network matching 50 Ω to 30 Ω and a 95-Ω miniature transmission line, and at higher frequencies, the line could be printed on the circuit board. The carrier frequency of 25 MHz made it possible to build components easily and to measure impedances of the first three harmonics with a vector-impedance meter.

The input circuit is simple and noncritical. Transformers T_2 and T_3 multiply the input voltage by four. R_1 prevents charge buildup on the gate. The parallel-tuned output tank has a Q of 3. The rf choke delivers dc power through L_1 and T_1 so that it operates into a low impedance and it does not have to contend with harmonics.

The 125-ohm transmission line and 50-Ω load should produce a drain load line of $125^2/50$ or 312 Ω, but the measured load line was 280 Ω. The difference may have been caused by variations in the coaxial cable and impedance transformation by stray reactances. With the measured load-line resistance of 280 Ω and R_{on} of 45 Ω, the expected efficiency is 280/(280+90), or 75.5%. The power output of a single FET with this load line will be limited by the peak-current rating of 0.05 A. The maximum supply voltage and power output are consequently:

$$V_{DD\,MAX} = (0.05)(280)\pi/8(0.755) = 7.25\ V$$
$$P_o = 8(0.755)^2(7.25)^2/280\pi^2 = 86.5\ mW$$

This load line is much more suitable to a pair of FETs. If the saturation voltages are equal, the equivalent R_{on} is half that of a single FET. For an R_{on} of 22.5 Ω, the pre-

Evaluating class F operation

Class F operation of a power amplifier in a high-frequency transmitter provides 27% higher efficiency and 27% higher output power than class B. A quick comparison with class C is difficult because class C amplifiers are operated with many different conduction angles and varying degrees of saturation.

The efficiency of an amplifier in Class C operation can be increased by decreasing the conduction angle toward zero. But since the power output decreases when the conduction angle is decreased, class C operation provides high efficiency only when output power is low. Class F operation, however, provides the high efficiency at high output power.

The field-effect transistor in the circuit of Fig. 1 would operate as a conventional class B amplifier if the transmission line were removed. In that mode, the FET is driven to act as a current source instead of a switch. The parallel-tuned output causes the drain voltage to be sinusoidal. For maximum efficiency, the drive voltage is adjusted so that the drain voltage swings from 0 to +2 V_{DD}. By analysis similar to that for the class F operation, the efficiency for class B is found to be

$$\eta_B = (\pi/4)[R/(R+2R_{on})] = 0.785\eta_F$$

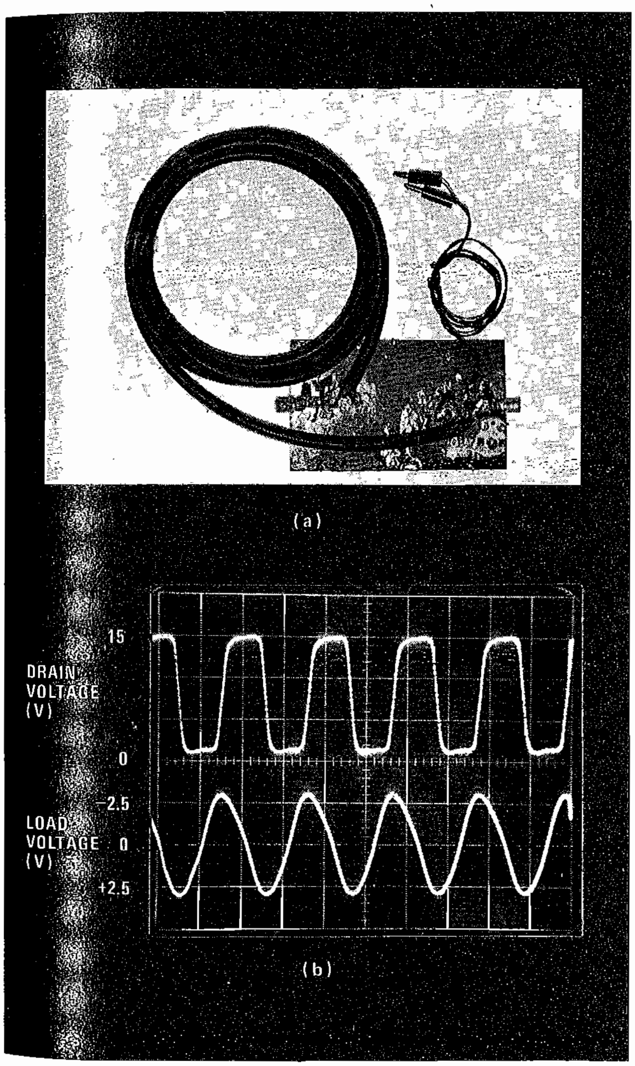
When R_{on} is zero, the class F circuit has an efficiency of 100%, and this equation yields the 78.5% maximum efficiency of class B operation.

dicted efficiency is 86%, and the power output is 332 mW. The FETs must have the same saturation resistances, or else the current must be divided equally by matching resistors or a current transformer.

If the same FET were operated in class B with the same load line, its efficiency would be only 59.3% and its power output 53.5 mW. A pair of FETs operated in class B would have an efficiency of 67.5% and an output of 205 mW.

The SD-200 performs well as a switch, as shown by the waveforms in Fig. 3b. The FET showed no tendency to oscillate during transition, and no neutralization circuitry was required. Any tendency to oscillate is reduced by operating as a switch because the FET has no gain when saturated or cut off.

The measured performance of the amplifier is shown in the five graphs of Fig. 4. Graph 4a shows output power as a function of supply voltage. Agreement with theoretical calculations is very good. Graph 4b shows



3. Model operation: Actual circuit (a) has input circuits and FETs on the left, output tuning and dc feed on the right. Transmission line T_1 is obvious. Voltage waveforms (b) correspond to those in Fig. 2. To miniaturize, a transmission line could be printed on the circuit board or approximated by discrete elements.

that efficiency is nearly constant for all supply voltages, except for a slight tendency toward higher efficiency at lower outputs. The single FET achieved an efficiency of about 71% at 86 mW output, which is nearly the predicted 75.5%.

By using two FETs, efficiency was improved to 73%. Why the efficiency did not improve as much as predicted is not known. Possibly, the current did not divide equally, which would have made equivalent R_{on} larger than expected. But when both one and two FETs were used, the class F amplifier exceeded the theoretical efficiency and power output for class B operation.

This type of amplifier has excellent amplitude-modulation characteristics, as shown in graph 4c. Output voltage v_{LP} varies linearly with supply voltage V_{DD}, except when the single FET exceeds its ratings (above V_{DD} of 7 V). The drive voltage was the same for all values of V_{DD}. This useful property of class F amplifiers results from using the drive to operate the device as a switch. In a class B or C amplifier, the FET acts as a current (or voltage) source, and both the drive and supply voltages must be modulated.

Feedthrough from the gate was negligible, even at the lower output levels. Since efficiency at reduced outputs is at least as high as it is at maximum power output, the efficiency of a modulated amplifier is at least as high as that of a continuous-wave amplifier. This is not true of a transistorized amplifier, where the saturation voltage becomes more significant at low outputs.

Graphs 4d and 4e demonstrate that this type of amplifier does not require critical adjustment. Although it is certainly not a broadband amplifier, it can be operated over a 10% bandwidth with negligible loss in efficiency. The peak drive voltage was held constant at 17 V at the gate, and 17/4 V at the input, for all of the previous data, but it could have been decreased by 6 dB without significant loss in efficiency.

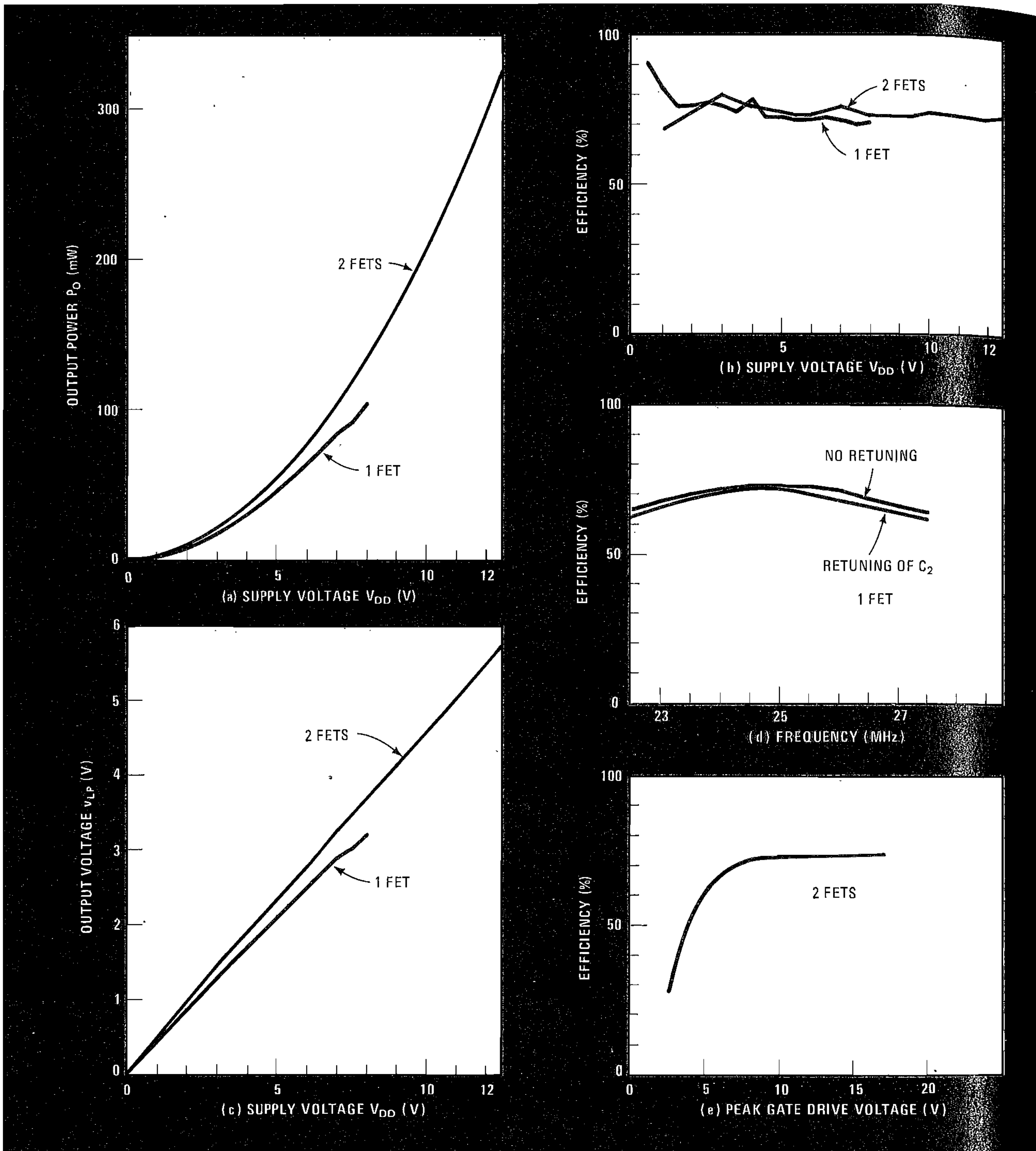
Refining the design

Higher efficiencies may be obtained by using a value of R larger than R_{MP}, but then the output is less than maximum. The use of R less than R_{MP} lowers both the efficiency and the output power.

The desired drain-load line can be produced in a variety of ways. If the parallel-tuned output were replaced by a π-network, the input impedance of the π-network and the characteristic impedance of the transmission line would then determine R. As an alternative, broadband transformers might be used. The transmission line must have essentially the same propagation velocity for at least the fundamental through the fourth harmonic. Coaxial cable is satisfactory, but 300-Ω television-antenna lead-in is not.

The carrier frequency must be low enough that switching occurs in a small fraction of a cycle so that, generally, the carrier frequency should not exceed about one tenth of the unity-gain frequency of the device.

The SD-200 has a unity-gain frequency higher than 1 GHz, so operation is possible at frequencies above 100 MHz. The SD-202 could be used at even higher frequencies, but it has a lower output. Capacitance at the



4. Graphic display. Measured performance of 25-MHz class F amplifier is shown in family of curves for a single FET and for two FETs in parallel. The nearly constant efficiency with varying output is demonstrated in (b), while modulation linearity is apparent in (c). Performance over a 10% bandwidth is shown in (d), and insensitivity to drive variations in (e). New V-MOS FETs can provide greater rf output.

drain should be kept to a minimum because it impedes rapid switching.

Since the gate voltage required for saturation depends on the drain current at a particular instant, sinusoidal drive can be used. When the driving voltage is below about 1 V, the device is cut off. The characteristic curves suggest a peak voltage of at least 6 V. The SD-201 should not be used because the diode protection will interfere with the driving signal. The gate capacitance may be included as part of the tank circuit of the previous stage. It should be possible to drive this amplifier from an oscillator or frequency multiplier with sinusoidal output, since negligible power is required.

Advances in FET technology will make it possible to extract higher output power from this type of circuit. For example, the recently-announced Siliconix VMP-1 V-MOS FET with a 50-Ω transmission line and a 30-V supply should produce about 12 W of rf output. □