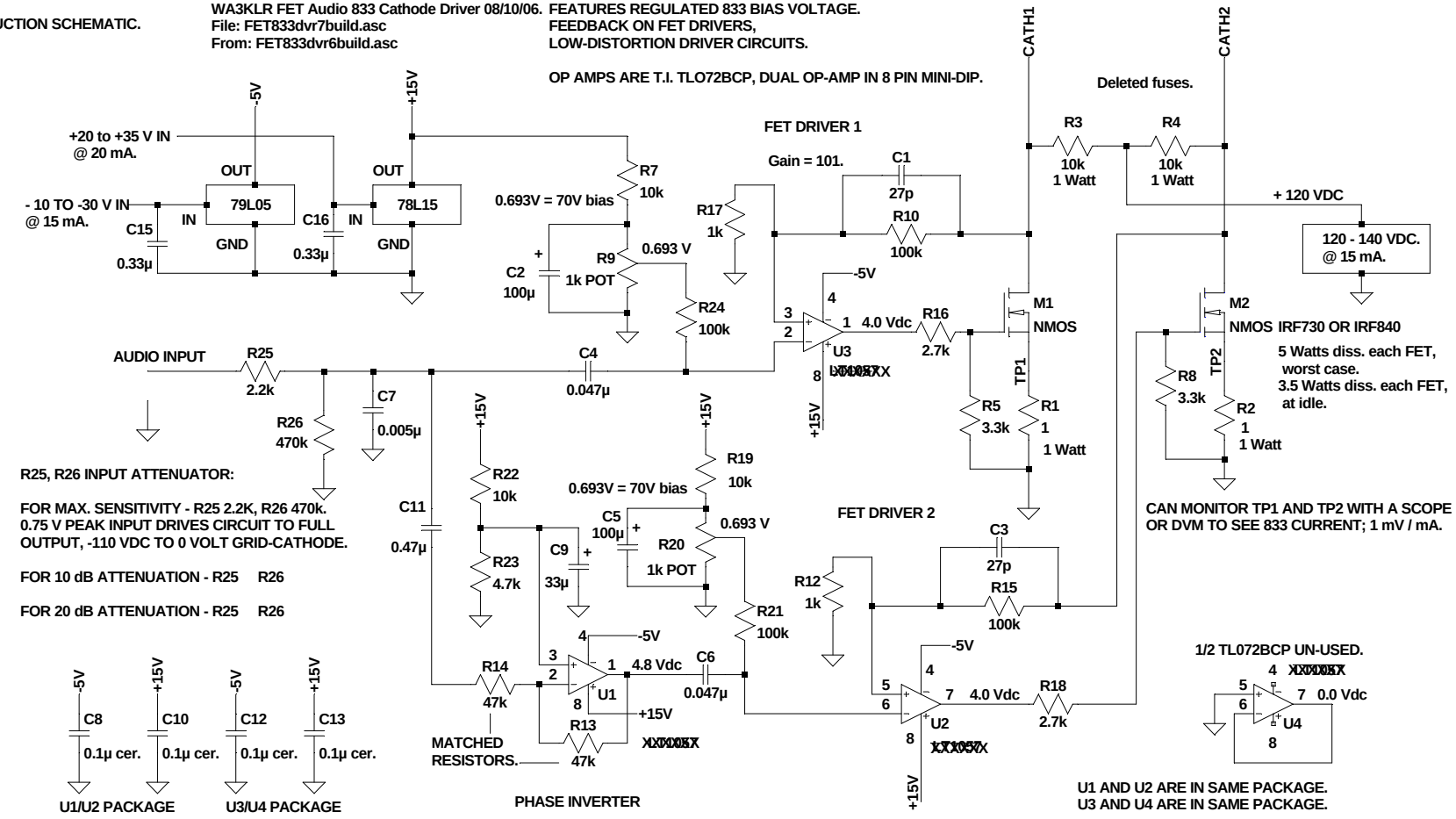
CONSTRUCTION SCHEMATIC.

WA3KLR FET Audio 833 Cathode Driver 08/10/06.
File: FET833dvr7build.asc
From: FET833dvr6build.asc

FEATURES REGULATED 833 BIAS VOLTAGE.
FEEDBACK ON FET DRIVERS,
LOW-DISTORTION DRIVER CIRCUITS.

OP AMPS ARE T.I. TLO72BCP, DUAL OP-AMP IN 8 PIN MINI-DIP.



START-UP:
CHECK REGULATOR INPUTS AND OUTPUTS, +120V FOR SHORTS TO GROUND.
RUN PCB ASSEMBLY BY ITSELF WITH THE +15 V, - 5 V, AND +120 V SUPPLIES ON. SET THE 2 BIAS POTS (R9, R20) FOR 0.693 VOLTS DC OUTPUT.
CHECK THAT THE 4 OP-AMP OUTPUT'S DC VOLTAGES ARE APPROXIMATELY AS NOTED ON SCHEMATIC ABOVE. U3-1 AND U2-7 OUTPUT VOLTAGE VARIES DEPENDING ON FET TYPE USED.

DC GAIN TRIM -
SET THE 2 BIAS POTS TO 1.000 VDC OUTPUT. JUMPER THE POT OUTPUTS TOGETHER WITH A CLIP LEAD.
BOTH CATHODE OUTPUTS CATH1, AND CATH2 SHOULD BE 101 VDC.
WHICHEVER CATHODE OUTPUT VOLTAGE IS LOWER, IT'S DC LEVEL MUST BE RAISED TO MATCH THE OTHER CHANNEL'S OUTPUT LEVEL.
PLACE A LARGE VALUE RESISTOR ACROSS THE 1K RESISTOR (R12 OR R17) OF THE CHANNEL THAT HAS THE LOWER VOLTAGE OUTPUT. MATCH OUTPUTS AS CLOSE AS POSSIBLE.

REMOVE CLIP LEAD FROM POTS. SET EACH POT FOR +70 VDC AT CATHODE OUTPUT.
DRIVE AUDIO INPUT WITH ENOUGH LEVEL TO GET NEAR MAXIMUM SINE WAVE OUTPUT SWING WITH NO DISTORTION. THIS SHOULD BE ABOUT 75 V PK-PK OUT FOR ABOUT 0.8 V PK-PK (280 mV RMS) IN.
READ THE AC RMS VOLTAGE OUTPUT OF BOTH CHANNELS, ABOUT 26 V. RMS. BOTH CHANNELS SHOULD READ VERY CLOSE TOGETHER. IF NOT, PHASE INVERTER GAIN MAY NOT BE EXACTLY -1.

SYSTEM OPERATION :
LEAVE BOARD ENERGIZED IN STANDBY MODE SO THAT IT IS STABILIZED WHEN MODULATOR PLATE SUPPLY IS KEYED.

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